FACULTY PROFILE ON WEBSITE

Faculty Name	**Dr.Vasudeva G**	
Academic Designation	**Assistant Professor**	
Educational Qualification	**BE, M. Tech, Ph.D**	
Experience in Teaching & Industry	**14 Years & 6Months**	
Date of Joining	**07/01/2022**	
Official Email ID	**Vasudeva-ece@dsatm.edu.in**	
Employee ID	**180549**	

Educational Details

1.Ph.D. from Visvesvaraya Technological University, Belagavi in the field of SAR based ADC Design (RVCE research Centre) and completed in the year 2022.

2. M.Tech in VLSI Design and Embedded systems studied at JSS academy of technical education, Bangalore. Secured First class and passed in the year 2008.

3. B.E. in Electronics and Communication Engineering department at Nagarjuna college of Engineering and technology, Bangalore. Secured First class and passed in the year 2006.

Professional Experience

1. Presently Working as Assistant Professor in the department of ECE at Dayananda Sagar Academy of Technology and Management, Bangalore from January 2022 to till date.

2. Worked as Assistant Professor in the department of ECE at Atria Institute of technology, Bangalore from July 2016 to June 2020.

3. Worked as Assistant Professor in the department of ECE at RV College of Engineering, Bangalore from September 2013 to March 2015.

4. Worked as Assistant Professor in the department of ECE at ACS College of Engineering, Bangalore from July 2012 to September 2013.

5. Worked as Lecturer in the department of ECE at Rajiv Gandhi Institute of technology, Bangalore from August 2009 to July 2012.

Publications

1. V. G *et al*., "Design and Development of UART Communication Over RSA Encryption," *2025 International Conference on Electrical and Computer Engineering Researches (ICECER)*, Antananarivo, Madagascar, 2025, pp. 1-6, doi: 10.1109/ICECER65523.2025.11401365.

2. Gowdagere, V., & Venkataramanaiah, U. B. (2022). Operational transconductance amplifier-based comparator for high frequency applications using 22 nm FinFET technology. International Journal of Electrical & Computer Engineering (2088-8708), 12(2), 2158.

3. Vasudeva, G., Jatkar, M., Kulkarni, T. R., Kulkarni, R. R., Gururaj, B., & Tejas, M. P. (2023). Design of FinFET Based Op-Amp Using High-K Device 22 nm Technology. In *Applied Mathematics, Modeling and Computer Simulation* (pp. 928-939). IOS Press.

4. Tripti R, K., Arun Vikas, S., Vasudeva, G., & Bharathi, G. (2025). Sanitization and Sterilization Robot Ultra Violet Based. *International Journal of Trend in Scientific Research and Development*, *9*(2), 1004-1010.

5. Vasudeva, G., Mallikarjun, P. Y., Jatkar, M., Kulkarni, T. R., Kulkarni, R. R., Gururaj, B., & Tejas, M. P. (2023, November). Design of OPAMP Based on 22 nm FinFET Technology. In *International Conference on Trends in Computational and Cognitive Engineering* (pp. 371-382). Singapore: Springer Nature Singapore.

6. Vasudeva, G., Mallikarjun, P. Y., Kulkarni, T. R., Bhuvan, M., Gowthami, K., & Nidhi, N. (2025). Design and optimisation of 3-bit flash ADC with low power double tail comparator. In *Engineering Science and Technology: Innovations for the Future* (pp. 220-226). CRC Press.

7. Vasudeva G, GURURAJ, B., LUTIMATH, N., & KULKARNI, T. (2024). CMOS Comparator Design using 90nm Technology. *ENGINEERING WORLD Учредители: World Scientific and Engineering Academy and Society*, *6*, 291-297.

8. Vasudeva, G., & Uma, B. V. (2021). Low voltage low power and high speed OPAMP design using high-K FinFET device. *WSEAS Transactions on Circuits and Systems*, *20*, 80-87.

9. Vasudev, G., & Hegadi, R. (2012). Design and development of 8-bits fast multiplier for low power applications. *International Journal of Engineering and Technology*, *4*(6), 774.

10. Vasudeva, G., & Uma, B. V. (2022). Design and Implementation of High Speed and Low Power 12-Bit SAR ADC Using 22nm FinFET. *Iranian Journal of Electrical & Electronic Engineering*, *18*(3).

11. Vasudeva, G., & Uma, B. V. (2021). 22nm FINFET based high gain wide band differential amplifier. *International Journal of Circuits, Systems and Signal Processing*, *15*, 55-62.

12. Vasudeva, G., Jatkar, M., Kulkarni, T. R., Kulkarni, R. R., Gururaj, B., & Tejas, M. P. (2023). Design of FinFET Based Op-Amp Using High-K Device 22 nm Technology. In *Applied Mathematics, Modeling and Computer Simulation* (pp. 928-939). IOS Press.

13. Jatkar, M., G, V., Kulkarni, T.R. et al. LC oscillator frequency prediction using machine learning linear regression algorithm. Discov Electron 2, 52 (2025). https://doi.org/10.1007/s44291-025-00092-9.

14. Shankar, G. V., & Girish, J. R. (2016). Design of High Performance CMOS Comparator using 90nm Technology. *International Journal of Modern Trends in Engineering and Research*, *3*(5), 333-337.

15. Vasudeva, G., & Raj, P. C. P. (2015). Study of 8 bit fast multipliers for low power applications.

16. Kulkarni, T.R., Vasudeva, G., Renukaprasad, G., Roopa, K.R., Srividya, B.V., Jatkar, M. (2026). Speech Detection of Pathological Voice Disorders Non-Invasively Using Machine Learning Algorithms. In: Joshi, A., Ragel, R.G., S., K. (eds) ICT: Applications and Social Interfaces. ICTCS 2025. Lecture Notes in Networks and Systems, vol 1874. Springer, Cham. https://doi.org/10.1007/978-3-032-19681-1_2.

17. Lutimath, Nagaraj M. and H. N, Divya and Gatti, Ravi and G, Vasudeva and B. K, Byregowda, Prediction of Heart Disease Using Hybrid Gaussian Naïve Bayes Technique (October 14, 2023). Proceedings of the International Conference on Innovative Computing & Communication (ICICC 2024), Available at SSRN: https://ssrn.com/abstract=4602168 or http://dx.doi.org/10.2139/ssrn.4602168.

18. Gururaj, B. (2023). Design of Modified Booth's Encoder Using SPST technique. International Journal of Electrical Engineering and Computer Science, 5, 73-86.

19. Vasudeva, G., Uma, B.V. (2022). Two-Stage Folded Resistive String 12-Bit Digital to Analog Converter Using 22-nm FINFET. In: Karrupusamy, P., Balas, V.E., Shi, Y. (eds) Sustainable Communication Networks and Application. Lecture Notes on Data Engineering and Communications Technologies, vol 93. Springer, Singapore. https://doi.org/10.1007/978-981-16-6605-6_8

20. Kulkarni, T.R. et al. (2026). Modeling Subthreshold Leakage in MOSFETs: Supervised Regression with Noise-Aware Synthetic Datasets. In: Senjyu, T., Mahmud, M., Joshi, A. (eds) Smart Trends in Computing and Communications. SmartCom 2026. Lecture Notes in Networks and Systems, vol 1990. Springer, Cham. https://doi.org/10.1007/978-3-032-26908-9_42.

21. PY, M., Khanderao, M. S., & Gururaj, B. (2026). Design and Implementation of DAC and Comparator using MOSFET. Grenze International Journal of Engineering & Technology (GIJET), 12(Part2), 1400.

22. PY, M., Gururaj, B., Kulkarni, T. R., MM, H., & HJ, A. (2026). RTL to GDSII Implementation of UART Communication Over RSA Algorithm using 90nm Technology. Grenze International Journal of Engineering & Technology (GIJET), 12(Part2), 4286.

23. GURURAJ, B. (2025). Design of an Efficient Single Precision Floating Point Unit. INTERNATIONAL JOURNAL, 7, 44-54.

24. Vasudeva, G., & Gururaj, B. (2024). Embedded Hamming Scheme Implementation Using Single Bit Error Detection and Correction. In Applied Mathematics, Modeling and Computer Simulation (pp. 550-557). IOS Press.

25. Vasudeva, G., & Gururaj, B. (2023). Low Noise Operational Amplifier using Current Driving Bulk by CMOS Technology. WSEAS Transactions on Electronics, 14, 144-149.

26. GURURAJ, B. (2025). Design of an Efficient Single Precision Floating Point Unit. INTERNATIONAL JOURNAL, 7, 44-54.

27. Banappa, H. S., Hemanth, S., Vignesh, S., Shivaji, C., & Vasudeva, G. FPGA Implementation of Chinese Remainder Theorem Over Residue Modulo.

28. Siddesh, B. H. M. Additive Multiply Module Architecture for Low Power 8-Bit Multipliers in VLSI.

International Conferences:

1. G. A. Vatsala, Fathimunnisa, M. S. Mudassir, G. Vasudeva, P. Jyothi and D. C. Rudresha, "SmartBinX: A Cost-Effective Hybrid AI and SensorBased Autonomous Waste Sorting System for Public Spaces," 2025 International Conference on Computational Innovations and Sustainable Technologies (ICCIST), Bangalore, India, 2025, pp. 1-6, doi: 10.1109/ICCIST67338.2025.11438295.

2. K. Roopa, T. Vignesh, B. Talukdar, M. Jatkar, G. Vasudeva and T. R. Kulkarni, "Optimized Test Vector Generation and Detection of Bridging Faults in Reversible Circuits with Cryptographic Validation," 2025 International Conference on NexGen Networks and Cybernetics (IC2NC), Erode, India, 2025, pp. 32-37, doi: 10.1109/IC2NC67409.2025.11376017.

3. Lutimath, N.M. et al. (2026). Classification of Flower Using Transfer Learning with Enhanced MobileNetV2. In: Swaroop, A., Virdee, B., Correia, S.D., Polkowski, Z. (eds) Proceedings of Data Analytics and Management. ICDAM 2025. Lecture Notes in Networks and Systems, vol 1690. Springer, Cham. https://doi.org/10.1007/978-3-032-08859-8_39.

National Conferences:

1. Participated and Presented a paper in the National Conference on "Recent Trends In Communication Technology" held at Karnataka State Higher Education Council,Palace Road,Bengaluru-560001 in Association With Centre for Industrial Computers Tumkur university sponsored by Karnataka state Higher Education Council on 13th Jan 2012.Attended from Rajiv Gandhi Institute of Technology,Bangalore.Paper titled: "Design and realization of Low Noise Operational Amplifier with current Driving Bulk using CMOS technology"
2. Participated and Published a Paper entitled "Study of Design and Development of 8-Bit Fast Multiplier for Low Power Applications" in the two days National Conference on "ADVANCED COMMUNICATION TRENDS" ACT 2012 on 23rd & 24th August 2012.
3. Participated and Presented a paper at National Conference on Emerging Trends in VLSI Design and Embedded Systems (ETVDES) Conference on 25th October 2013, attended from R V College of Engineering, Bangalore, Conducted at BMS INTITUTE OF TECHNOLOGY, Yelahanka, Bangalore-64, Titled "Design of Radix-2 Modified Booth's Encoder using FPGA and ASIC Methodology". Co-Author: Prof. J.R. Girish from SJB INSTITUTE OF TECHNOLOGY, Bangalore.

Conference Attended

1. Attended an International conference-ICWITE-2025 as a session chair at BGSIT Bangalore.
2. Attended an International conference ICECER-2025 in offline mode.
3. Attended an International conference ICEEECS-2025 in offline mode.

Awards

1. Received a certificate from DSATM College as Best professional performer for the year 2025.

Academic Activity

1. Coordinating to Handle NAAC 2 criteria files and NBA 6 criteria files.
2. Working as a Library coordinator at department level.

Faculty Development Activity/Workshops

1. Attended a 2-Day workshop at REVA Institute of Technology and Management, Kattigenahalli, Yelahanka, Bangalore-64 on "VLSI DESIGN VERIFICATION" on 29th July and 30th July 2010 from Rajiv Gandhi Institute of Technology, Bengaluru.

2. Attended a 3-Day Training Program from 3/1/2012 to 5/1/2012 on "Analog and Digital Design" held at Cadence Design Systems, Bangalore.

3. Participated in the 4-Day VTU-VGST Faculty Development Program from ACS College of Engineering, Bangalore on "VLSI System on Chip and Validation" from 10th July 2013 to 13th July 2013 Organized by R & D Centre and ECE Department, M.S.Engineering College, Navarathna Agrahara,Sadahalli Post ,off Bangalore International Airport Road,Bangalore562110.

4. Participated in 5-Day workshop from RV College of Engineering, Bangalore on "Faculty Pedagogical Development Programme" Organized by International Academy for Competency Enhancement, Bangalore from 15/7/2014 to 19/7/2014.

5. Participated in the Workshop on "Geospatial Technology and its Applications" from RV College of Engineering, Bangalore from 4th -6 th December 2013 as a part of Institution Academic Networking Programme under TEQIP-II from Sir M Visvesvaraya Geospatial Chair, Indian Institute of Science, Department of Civil Engineering, Information Science and Instrumentation Technology, Rashtreeya Vidyalaya College of Engineering(RVCE) and Karnataka State Council for Science & Technology(KSCST).

6. Attended a Faculty Development Programme on "Personality Development" Conducted by Department of Management Studies & Research on 22nd & 23rd July 2015 at Don Bosco Institute of Technology, Kumbalagodu, Mysore road, Bangalore-560074.

7. Attended a Faculty Development Programme on "Physical Design challenges in DSM Node VLSI Systems", Organized by Department of Electronics and Communication Engineering, B.N.M. Institute of Technology, Bengaluru, -560070, during 16th to 21st January 2017

8. Attended a Faculty Development Programme at Hotel Atria, Bangalore on "Pedagogy training".

9. Attended a Faculty Development Programme on "Latest Trends In Wireless Communiction" Organized by Department of Electronics and Communication Engineering , in association with Jetking Sadashivnagar , held on 24th July 2017 at Atria Institute of Technology,Bengaluru560024

10. Attended a Faculty Development Programme on "IOT and Embedded Systems" Organized by Department of Electronics and Communication Engineering , Atria Institute of Technology ,Anandnagar,Bengaluru-560024 , Karnataka during 22nd to 27th January 2018.

11. Attended a one week workshop on “RTOS and Machine Learning in the Edge Devices” held on 14th Jan 2019 to 19th Jan 2019 organized by the Department of Electronics and Communication Engineering ,Atria Institute of Technology, Bangalore-24.

12. Attended a 2-Day workshop on “VLSI design flow using Xilinx Vivado” held from 28th to 29th January 2019,organized by the Department of Electronics and Communication Engineering, Atria Institute of Technology,Bengaluru-24.

13. Attended a online Workshop Conducted by Department of Electronics and Communication Engineering, TEQIP(Phase-III) Sponsored on “Recent Trends in VLSI Devices/Circuits and Applications” held at Malaviya National Institute of Technology,Jaipur, from 1st October to 5th October 2020.

14. Attended a online workshop Conducted by Department of Electronics and Communication Engineering ,TEQIP(Phase-III) Sponsored Five Days from 26th November 2020 to 30th November 2020 on “Emerging CMOS Technologies and Beyond: Trends and Challenges” held at Malaviya National Institute of Technology,Jaipur.

15.Participated in 5 days FIP on “Empowered Teachers as the torch bearers and pedagogical leaders” organized by Teaching Learning Center, DSATM, Bengaluru., from 26th Feb to 1st March 2024.

16. Participated in NPTEL-AICTE FDP on “Outcome Based Pedagogic Principles for Effective Teaching” organized by Indian Institute of Technology, Kharagpur, from Feb-Mar 2023 (4-week Course).
17. Completed NPTEL online certification course on Introduction to Machine Learning .
18. Completed NPTEL online certification course on CMOS VLSI Design.
19. Completed NPTEL online certification course on VLSI Physical Design,
20. Completed NPTEL online certification course on Artificial Intelligence: Concepts and Techniques.
21. Completed NPTEL online certification course on Semiconductor Devices and Circuits.
22. Completed NPTEL online certification course on VLSI Design Flow: RTL to GDS.

Contact Details

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